III. Remarks

Applicants are grateful to the Examiner for allowing Claims 1-28 and 32. Reconsideration and withdrawal of the rejection of Claims 29-31 and 33-34 are respectfully requested in view of the following arguments and the foregoing amendments.

A. Rejection under 35 U.S.C. § 102

The Action rejects Claims 29 and 31 as being unpatentable over the Admitted Prior Art by Applicant (APA). Reconsideration and withdrawal of this rejection in view of the following arguments are respectfully requested.

FIG. 1 of APA illustrates a cross-sectional view of an active region of a field effect transistor formed on a SOI substrate in accordance with the prior art. The method of forming the structure of FIG. 1 includes forming a silicon layer on a substrate 100 having an oxide isolation layer 110 formed thereon; forming a cap dielectric layer (not shown) on the silicon layer; patterning the cap dielectric layer and the silicon layer to define an active silicon region 120; forming a thermal oxide layer (not shown) only on the sidewalls of the active region 120; and removing the cap dielectric layer. During the cap dielectric layer removal step, a portion of the isolation layer 110 is also removed, and undercut regions 125 are formed beneath the active region 120. Sometimes, a subsequent process for cleaning the substrate prior to forming a gate dielectric layer also contributes to the loss of the isolation layer 110 and further extends the undercut regions 125 beneath the active region 120. This undercut can lead to structure collapse.

Applicants agree with the Examiner, as argued in the previous response, that the recitation of the "isolation layer being **substantially without undercut** at the region within the isolation layer beneath the conductive region" allows for some undercut of the isolation layer, but it does not allow for substantial undercuts. The description of FIG. 1 from the APA provides that undercut 125 shown in FIG. 1 can cause serious defects in the device, such as structure collapse, leading to lower production yields. Certainly then, FIG. 1 of APA shows undercuts

125 that are "substantial" as they create structural problems for conductive region 125. It follows, therefore, that the structure of FIG. 1 is not "substantially without undercut" as claimed.

Reconsideration and withdrawal of the rejection of Claim 29, therefore, are respectfully requested.

The Action also rejects Claim 31, which recites that the conductive region has a "mesa structure," as being anticipated by APA. Applicants submit that it has distinguished a non-mesa structure (rectangular element 120 of APA FIG. 1 having vertical sidewalls) from a mesa structure (trapezoidal element 225 of FIG. 2G) in the present application. As explained in ¶15 of the present application, providing conductive regions with a mesa structure or shape provides advantages for subsequent processing, such as improved etch margin for pattering the gate and/or the enhanced filling ability of an interlayer dielectric (ILD) between active regions. Clearly, the rectangular shape of element 120 of APA FIG. 1 is not a "mesa structure" as defined by Applicants.

For at least these additional reasons, it is submitted that Claim 31 is allowable over the art of record. Reconsideration and withdrawal of the rejection of Claim 31 are respectfully requested.

B. Claim Rejection under 35 U.S.C. §103(a)

1. Claim 30

The Action rejects Claim 30 – which recites that any undercut within the isolation layer has a lateral depth of no more than about 100Å – as being obvious from the APA. The Examiner's basis for this rejection is that it would have been obvious to select this depth "since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable range involves on routine skill in the art." (citing *In re Aller*). Applicants respectfully submit that the Examiner's reliance on *In re Aller* is misplaced.

The amount of the undercut was not controllable in any practical sense, before Applicants' invention. As set forth in the APA, Before Applicants invention, it was not possible to control the undercut of the isolation layer in the region of the conductive element 125. The etching processes employed to remove the cap dielectric layer(s) as well as post-etching cleaning processes undercut the isolation layer. It is submitted that the "general conditions of the claim" are not present in the prior art because this undercut was not controllable. Therefore, it could not be obvious to one of ordinary skill at the time of invention to select this lateral depth to be 100Å or less, as suggested by the Examiner.

To arrive at such a limitation, one of ordinary skill would have to employ, for example, a process as set forth in Claim 1, which the Examiner has conceded is allowable. Therefore, it is respectfully submitted that the limitation of Claim 31 that any undercut within the isolation layer has a lateral depth no more than about 100Å can only come from Applicants' disclosure of their invention and is not, therefore, obvious from the APA. Therefore, it is submitted that Claim 30 is allowable over the APA. Reconsideration and withdrawal of the rejection of this claim are respectfully requested.

2. Claims 33-34

The Action rejects Claims 33-34 as being obvious from the U.S. Patent No. 6,562,665 to Yu in view of U.S. Patent No. 6,489,201 to Yoon.

Claim 33 has been amended to recite a step (e) of "after said cleaning process, and before said gate dielectric forming step, removing remaining portions of the sacrificial dielectric layer." Claim 33 now clearly requires that the sacrificial dielectric layer remains to protect the isolation layer from undercut during the cleaning step and that portions remaining after the cleaning step are then removed.

In relying on Yu, the Examiner cites to layers 328 and 334 as being sacrificial dielectric layers. As shown in FIG. 11 to FIG. 12 of Yu, the first spacers 328, second spacers 334 and cap layer 310 are etched away to leave pillar 314 on the buried insulator layer 302. Yu does not

provide that at least a portion of these layers remain during any subsequent cleaning process, or that such portions are then removed prior to formation of the gate dielectric after the cleaning process.

Whether Yoon teaches a cleaning process as argued by the Examiner is of no consequence, as the combination of reference still would not teach the combined steps of: (1) forming a sacrificial dielectric layer over the isolation layer and adjacent to said at least one conductive region; (2) performing a cleaning process prior to forming said gate dielectric layer, wherein said sacrificial dielectric layer is formed to a thickness sufficient to substantially protect said at least one conductive region from undercut in the isolation layer from said cleaning process; (3) after said cleaning process, and before said gate dielectric forming step, removing remaining portions of the sacrificial dielectric layer; and then (4) forming a gate dielectric layer over said at least one conductive region.

Therefore, the combination of references does not teach each feature claimed in Claim 33. It is submitted, therefore, that Claim 33 and Claim 34, which depends from Claim 33, are allowable over the art of record. Reconsideration and withdrawal of the rejection of these claims in view of the foregoing amendments and arguments are respectfully requested.

PATENT

ATTORNEY DOCKET NO.: N1085-00192
[TSMC2003-0289]

IV. Conclusion

In view of the foregoing remarks and amendments, Applicants submit that this application is in condition for allowance at an early date, which action is earnestly solicited.

The Commissioner for Patents is hereby authorized to charge any additional fees or credit any excess payment that may be associated with this communication to deposit account **04-1679**.

Respectfully submitted,

Dated: 7/13/05

Joseph A. Powers, Reg. No.: 47,006
Attorney For Applicants

DUANE MORRIS LLP
One Liberty Place
Philadelphia, Pennsylvania 19103-7396
(215) 979-1842 (Telephone)
(215) 979-1020 (Fax)